REMARKS/ARGUMENTS

In response to the Office Action dated July 9, 2003, claims 1, 9, and 21 are amended. Claims 1, 2, 4, 6, 7, 9-14, 17-19, 21-28, and 32-34 remain in the application. It is not the Applicants' intent to surrender any equivalents because of the amendments or arguments made herein. Reexamination and reconsideration of the application are respectfully requested.

Art-Based Rejections

On pages 2-3 of the Office Action, claims 1-2,4, 6, 14, 17-18, 26-28, and 32-34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nakada et al., JP 63175490.

On pages 3-4 of the Office Action, claims 7, 9-13, 19, and 22-25 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakada et al., JP 63175490 in view of Kawamura et al, USPN 6,452,880.

On page 5 of the Office Action, claim 21 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakada et al., JP 63175490 in view of admitted prior art.

The Applicant respectfully traverses the rejections in light of the clarifying amendments above and the arguments below.

The Nakada Reference

The Nakada reference discloses a semiconductor laser. A semiconductor laser is constituted in a structure, wherein a front end face 21 of a submount 20 is formed at a prescribed angle with an exit end face 11 of a laser chip 10 in such a way that the front end face 21 of the submount 20, whereon the laser chip 10 is mounted, and laser light

to be oscillated from the laser chip 10 do not intersect orthogonally from each other. See Constitution.

The Kawamura Reference

The Kawamura reference discloses an optical pickup apparatus having a 650 nm light emitting device and a 780 nm light emitting device (see Col. 6, lines 53-54).

The Admitted Prior Art

The admitted prior art discloses a diffraction grating, collimator lens, half mirror, objective lens, and a light receive element.

The Claims are Patentable over the Cited Reference

The claims of the present invention describe a semiconductor laser device. A device in accordance with the present invention comprises a semiconductor laser chip having a first surface of which shape is approximately rectangular or square, and having an emission facet for emitting a laser beam, and a sub-mount having a first surface on which the semiconductor laser chip is provided, and at least one second surface vertical to the first surface, the first surface of the sub-mount having parallel first edges and parallel second edges between the first edges, the second edges being inclined at an angle of 3 to 30 degrees to the first edges, the first edges being parallel to the edges of the first surface of the semiconductor laser chip, one of the second edges being corresponding to the emission facet, wherein the one second surface including one of the second edges corresponding to the emission facet inclines along with the at least one of the second edges and reflects an incident light orthogonal to the emission facet of the semiconductor laser chip to a different direction in accordance with the angle of the second surface.

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The cited references do not teach nor suggest the limitations of the claims of the present invention. Specifically, the cited references does not teach nor suggest the limitation of the first surface of the sub-mount having parallel first edges and parallel second edges between the first edges, the second edges being inclined at an angle of 3 to 30 degrees to the first edges as recited in the claims of the present invention.

In amended claims 1, 9 and 21, a first surface of a semiconductor laser chip has substantially a rectangle or square shape. Further, a first surface of a sub-mount comprises parallel first edges which are arranged to be parallel to the edges of the first surface of the semiconductor laser chip, and parallel second edges which are inclined at an angle of 3 to 30 degrees to the first edges. One of the second edges of the sub-mount is arranged in such a manner that an incident light orthogonal to the emission facet can be reflected to a different direction. According to such a structure, the sub-mount is in a parallelogram shape having parallel first edges and parallel second edges inclined at an angle of 3 to 30 degrees to the first edges. Thus, the sub-mount can be easily manufactured by dicing a wafer diagonally. As a result, the cost for manufacturing the sub-mount is reduced.

In Nakada et al., a sub-mount 20 of FIG. 1 does not have a front surface 21 and a rear surface 22 which are parallel to one another. Thus, Nakada et al. does not disclose a sub-mount 20 with parallel first edges and parallel second edges inclined at an angle with respect to the first edges as recited in the claims of the present invention. Further, the sub-mount 20 is manufactured by, for example, dicing a wafer in such a manner that a diced chip has an area which is twice the size of the sub-mount 20, and cutting the center portion of the diced chip at an angle of 5 degrees. Hence, with Nakada et al., it is difficult to manufacture the sub-mount 20 by simply dicing a wafer.

As such, Nakada does not teach nor suggest all of the limitations of independent claims 1, 9, and 21, namely, Nakada does not teach nor suggest the limitation of the

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first surface of the sub-mount having parallel first edges and parallel second edges between the first edges, the second edges being inclined at an angle of 3 to 30 degrees to the first edges as recited in the claims of the present invention, and therefore, claims 1, 9, and 21 are patentable over Nakada.

The ancillary Kawamura reference and the admitted prior art do not remedy the deficiencies of the Nakada reference, namely, the other references do not teach nor suggest the limitation of of the first surface of the sub-mount having parallel first edges and parallel second edges between the first edges, the second edges being inclined at an angle of 3 to 30 degrees to the first edges as recited in the claims of the present invention. Therefore, claims 1, 9, and 21 are patentable over the cited references under 35 U.S.C. §§ 102 and 103.

Thus, it is submitted that independent claims 1, 9, and 21 are patentable over the cited references. Claims 2, 4, 6, 7, 10-14, 17, 18, 19, 22-28, and 32-34 are also patentable over the cited references, not only because they contain all of the limitations of the independent claims, but because these claims also describe additional novel elements and features that are not described in the prior art. Silence with respect to the remainder of the arguments should not be taken to mean that the Applicant agrees with the arguments presented in the Office Action.

Conclusion

It is submitted that this application is now in good order for allowance and such allowance is respectfully solicited. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at telephone number (213) 337-6742 to discuss the steps necessary for placing the application in condition for allowance.

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If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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Date: February 5, 2004

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